7. (New) In the method of operating an analog to digital converter for resolution ement, the steps of:

displacing the span of the analog to digital converter along the vertical axis to one of a plurality of overlapping positions comprising shaded offset bands wherein the width of each band is representative of the span of the digital converter; and,

overlapping the offset bands to provide hysteresis.

Sub of Cont.

8. (New) A method for resolution enhancement in an analog to digital converter comprising the steps of:

converting a reference voltage of more than a least significant bit;

subtracting the converted reference voltage of more than a least significant bit from the input voltage; and then

adding the converted reference voltage of more than a least significant bit to the converted reduced input voltage.

REMARKS

The deficiencies pointed out in claims 1-5 in paragraph 2 of the Office Letter under 35 U.S.C. 112 were noted. An effort to provide proper antecedent basis including claim 6 has been made in the present amendment.

Claim 1 has been further amended to define the invention with antecedent support at page 9, line 21 through page 10, line 1 of the specification.

Claim 4 has been further defined with respect to the programmed gain preamplifier and having anetecedent support at page 10, lines 13-14 of the specification.

The reference patent *Sonu et al.*, 6,215,433 is directed to a solution for eliminating a low-frequency offset which adversely affects clock jitter. In the '433 patent, the clock is derived from the low frequency components of a demodulator output.

The *Sonu et al.* system relates to a DC sensitive clock generator and does not appear to show a method and apparatus for extracting a higher resolution digital value. *Sonu et al.* focuses on eliminating low frequency signals.

Accordingly, added method claims 7 and 8 are believed to distinguish over *Sonu et al.*

Antecedent basis for method claim 7 is found at least at page 9, lines 1-7 and lines 13-14 of the specification.

Claim 8 defines a method of resolution enhancement in an AC converter in a manner differing the present system over *Sonu et al.* and finding antecedent support at least at page 5 lines 13-17 of the specification.

In view of the preceding, it is believed that the claims proffered for the Examiner's consideration contain patentable subject matter, which Notice is respectfully solicited.

The fee for claims has been calculated as shown below:

	Claims Remaining After Amendment	**Highest No. Previously Paid For**	**Present Extra**	**Rate**	**Addi'l Fee**
Total	8	Minus 20	= 0	x $18 =	$0
Indep.	8	Minus 5	= 3	x $84 =	$252
[] First Presentation of Multiple Dependent Claim				+ $280 =	$0
Total Additional Fee					$252

Please charge Deposit Account No. 02-2960 in the amount of 252.00. The Commissioner is hereby authorized to charge any additional fees, including fees for extension of time, which

may be required at any time during the prosecution of this amendment without specific authorization, or credit any overpayment to Deposit Account 02-2960.

PETITION AND FEE FOR EXTENSION OF TIME
37 C.F.R. § 1.136(a)

The applicant petitions the Commissioner of Patents and Trademarks to extend the time for response to the office action dated June 28, 2001 for two months from September 28, 2001 to November 28, 2001.

Please charge the fee of $390.00 for 2 months to Deposit Account No. 02-2960. Please charge any necessary additional fees under 37 C.F.R. § 1.16 or § 1.17 or credit any overpayments to Deposit Account No. 02-2960.

Respectfully submitted,

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ATTACHMENT FOR SPECIFICATION AMENDMENTS

None.

ATTACHMENT FOR CLAIM AMENDMENTS

The following is a marked up version of amended claims 1-6 in which underlines indicate insertions and brackets indicate deletions.

1. (Amended) An analog to digital converter resolution enhancement method comprising the steps of:

providing an analog to digital converter having an AC component less than or equal to one-half the span of the analog to digital converter;

connecting the input signal [through] to the input of a programmed gain preamplifier;

utilizing [the] said programmed gain preamplifier to match the full range of [the] said analog to digital converter to [the] said AC component of the input signal; and then,

complementing the analog to digital [converter] range of said analog to digital converter by an offset value thereby causing [the] said programmed gain preamplifier to amplify the input signal at high gain while applying the offset value at low gain.

2. (Amended) An analog to digital converter having resolution enhancement comprising in combination:

an analog to digital converter having a full range and an input terminal and an output terminal;

a programmed gain preamplifier having an input terminal for receiving an input signal having an AC component portion and an output terminal coupled to the input terminal of said analog to digital converter;

said programmed gain preamplifier matching [the] said full range of said analog to digital converter to only [the] said AC component portion of the input signal;

said analog to digital converter having a range complemented by an offset value; and

a summing junction for combining the output of said analog to digital converter with said offset value thereby causing said programmed gain preamplifier to amplify the input signal at high gain while applying the offset value at low gain.

3. (Amended) A method for calibrating [the] an analog to digital converter having resolution enhancement [of claim 2] including the steps of:

calibrating the analog to digital converter for each of a plurality of offset values; and,

wherein calibrating for each of a plurality of offset values includes generating a corresponding plurality of calibration waveforms.

4. (Amended) In combination:

a reduced span analog to digital converter;

a programmed gain preamplifier coupled between an input terminal for receiving an input signal and said reduced span analog to digital converter;

said programmed gain preamplifier having a high differential gain for said input signal and a low single-ended gain for the offset signal;

said programmed gain preamplifier matching the span of said analog to digital converter against only a portion of the system input; and,

the entire input signal range provided by positioning the converter's span by means of an offset value.

5. (Amended) In combination:

a digital converter having an input terminal and an output terminal;

a programmed gain preamplifier having an input terminal for receiving an input signal, an offset terminal, and an output terminal;

a digital summing junction;

said output terminal of said analog to digital converter coupled to said digital summing junction;

an anti-alias filter having an input terminal and an output terminal;

said output terminal of said anti-alias filter coupled to said input of said analog to digital converter;

said input terminal of said anti-alias filter coupled to said output terminal of said programmed gain preamplifier; and,

[a] said digital to analog converter coupled between said digital summing junction and said offset terminal of said programmed gain preamplifier for providing an analog offset signal to said programmed gain preamplifier.

6. (Amended) The combination according to claim 5 wherein said programmed gain preamplifier provides a high differential gain for [the] said input signal and a low single-ended gain for said analog offset signal.